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control bus CB is provided which is allocated to both screen regions **312** and **314** and on which the clock and control signals are carried which are necessary for dual scan LCD visual display units and are known per se. For its part, the VGA controller **10** is driven via a further bus **14**, from the arithmetic unit **12** of a PC, which is otherwise not illustrated. The essential part of a VGA controller of this said type is, for example, the component No. 65535 "Flat Panel/CRT VGA Controller", from the company Chips and Technologies, Inc., to which only a VGA BIOS and a video replay memory now need be connected.

The present invention makes use of the characteristics of a "Flat Panel/CRT VGA Controller" of this said type. In this case, parts which occur more than once are given the same reference characters in the following text.

FIG. 1 shows a block diagram of the connection of two LCD visual display units **110** and **112**, which operate using a single scan method that is known per se, to a VGA controller **10** which is set up for the dual scan mode. The data input D of one visual display unit **110** is connected via the upper data bus UDB to the VGA controller **10**, and the data input D of the other visual display unit **112** is connected via the lower data bus LDB to the VGA controller **10**. The control bus CB is connected in parallel to the clock signal input C of the two visual display units **110** and **112**. The connection of the VGA controller **10** to an arithmetic unit **12** via a bus **14** is made in a corresponding manner to the prior art illustrated in FIG. 3.

In the case of mutually independent operation, the visual display units **110** and **112** may have a maximum format of 320×480 pixels, corresponding to 15×80 characters. In the text mode, the first fifteen lines of a frame are displayed on the visual display unit **110** which is connected to the upper data bus UDB, and the second fifteen lines of a frame are displayed on the visual display unit **112** which is connected to the lower data bus LDB. A corresponding situation applies to the graphics mode. However, commercially available smaller formats with, for example, 320×240 pixels, corresponding to 15 lines of 40 characters each, can also be connected, although they then only partially utilize the display capacity of the full format.

FIG. 2 shows a block diagram of the connection of four LCD visual display units **210**, **212**, **214** and **216**, which are operated using the single scan method, to a VGA controller **10** which is set up for the dual scan mode. The data inputs D of the visual display units **210** and **212** are connected via the upper data bus UDB to the VGA controller **10**, and the data inputs D of the visual display units **214** and **216** are connected via the lower data bus LDB to the VGA controller **10**. The clock signal inputs C of the visual display units **210** and **214** are connected directly to the control bus CB, while the clock signal inputs C of the visual display units **212** and **216** are connected to a control bus CB', upstream of which a gate circuit **218** having a counter is connected. This gate circuit **218** suppresses the clock signals for video information items which are displayed on the directly driven visual display units **210** and **214**.

In the case of mutually independent operation, the visual display units **210–216** may have a maximum format of 320×240 pixels, corresponding to 15×40 characters. In the text mode, positions 1–40 of lines 1–15 of a frame are displayed on the first visual display unit **210**, positions 41–80 of lines 1–15 are displayed on the visual display unit **212**, positions 1–40 of lines 16–30 are displayed on visual display unit **214**, and positions 41–80 of lines 16–30 are displayed on visual display unit **216**. The visual display unit

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210 thus forms the left-hand upper quarter of a frame, the visual display unit **212** forms the right-hand upper quarter, the visual display unit **214** forms the left-hand lower quarter, and the screen **216** forms the right-hand lower quarter. A corresponding situation applies to the graphics mode. Visual display units with a smaller format may also be connected. The display capacity of the full format is then only partially utilized.

If the left-hand visual display units **210** and **214** have a different number of character positions, a dedicated gate circuit must be assigned to each right-hand visual display unit, or a gate circuit having a plurality of outputs is used, which emit clock signals after the respectively required number of steps.

The VGA controller **10** is once again connected via a bus **14** to an arithmetic unit **12** in a corresponding manner to the prior art illustrated in FIG. 3.

The exemplary embodiments which have been explained with reference to FIGS. 1 and 2 can also be combined with one another, for example, a visual display unit having 15×80 characters, corresponding to 320×480 pixels, can be connected to the upper data bus UDB, and two visual display units having 15×40 characters, corresponding to 320×240 pixels each, can be connected to the lower data bus LDB. In the text mode, positions 1–80 of lines 1–15 of a frame are then displayed on the upper visual display unit, and positions 1–40 or 41–80 of lines 16–30 are displayed on the lower visual display units.

In all the examples, the visual display units may also have a larger format. The information intended for one screen then occupies only a portion of the screen area, while information which is also displayed on an adjacent visual display unit appears on the remaining area. This can be utilized in a simple manner for simultaneously displaying information on a number of visual display units. If this is not desired, it is necessary to suppress the relaying of the video data and clock signals relating to the last-mentioned information items.

The operation of a number of visual display units in the indicated manner from a single screen control unit **10** has the advantage that, instead of these visual display units, a single full screen may also be connected without the display programs having to be changed. When user programs are being created and tested, the contents of the visual display units **110**, **112** and **210–216** are displayed to the programmer as subareas on a single visual display unit. It is also possible to create and to test such programs on a PC with standard equipment, without the various visual display units having to be available. Similar advantages also result during the installation and maintenance of an installation whose visual display units under some circumstances are spread over a large area and therefore cannot be seen at a glance.

Although other modifications and changes may be suggested by those skilled in the art, it is the intention of the inventor to embody within the patent warranted hereon all changes and modifications as reasonably and properly come within the scope of their contribution to the art.

What is claimed is:

1. A method for independent operation of a plurality of visual display units from one screen control unit, comprising the steps of:

emitting clock signals and a number of character-related or pixel-related video data signals corresponding to line and column resolution of a two-dimensional rectangular raster image which is to be displayed on a full screen,